CLAIMS

What is claimed is:

1. A ball grid array device comprising:

a substrate, further including:

a first major surface; and

a second major surface; and

an array of pads made of an electrically conductive material, the array of pads positioned on the first major surface, at least one of the array of pads including a diffusion retarding layer to retard the rate of diffusion of the electrically conductive material from the pad.

2. The ball grid array device of claim 1 further comprising a binding layer for binding the diffusion retarding layer to the conductive material of the at least one pad.

3. The ball grid array device of claim 2 further comprising a layer of material for receiving solder.

4. The ball grid array device of claim 2 further comprising a layer of material for receiving solder placed on the diffusion retarding layer.

5. The ball grid array device of claim 1 wherein the electrically conductive of the pad includes copper.

6. The ball grid array device of claim 1 wherein the diffusion retarding layer includes Kovar®.

7. The ball grid array device of claim 1 wherein the diffusion retarding layer includes 54Fe-29Ni-17Co.

8. The ball grid array device of claim 2 wherein the binding layer includes Titanium (Ti).

9. The ball grid array device of claim 2 wherein the binding layer is Titanium (Ti).

10. The ball grid array device of claim 9 wherein the Titanium binding layer has a thickness in the range of 80 nanometers (nm) to 120 nanometers (nm).

11. The ball grid array device of claim 9 wherein the Titanium binding layer has a thickness in the range of 90 nanometers (nm) to 110 nanometers (nm).

12. The ball grid array device of claim 4 wherein the layer of material for receiving solder includes gold (Au).

13. The ball grid array device of claim 4 wherein the layer of material for receiving solder is gold (Au).

14. A substrate comprising:
at least one pad of a copper material;
a diffusion retarding layer placed over the at least one pad; and
a layer of gold over the at least one pad diffusion retarding layer.

15. The substrate of claim 14 wherein the diffusion retarding layer includes 54Fe-29Ni-17Co.

16. The substrate of claim 14 further comprising a layer of titanium (Ti) used to bond the diffusion retarding layer to the material of the at least one pad.

17. The substrate of claim 14 wherein the diffusion retarding layer

includes 54Fe-29Ni-17Co, the substrate further comprising a layer of titanium (Ti) used to bond the diffusion retarding layer to the material of the at least one pad.

18. The substrate of claim 14 further comprising a plurality of pads.

19. The substrate of claim 14 further comprising a plurality of pads arranged in an array.

20. A method for forming a pad on an electronic device comprising:
forming a copper pad on the electronic device; and
placing a layer of material to retard diffusion of the copper over the copper pad.

21. The method of claim 20 wherein placing a layer of material to retard diffusion of the copper into the solder ball further comprises adding a layer of material to bind the layer of material to retard diffusion of the copper.

22. The method of claim 21 further comprising placing a layer of a material to enhance the solderability of the pad onto the layer of material to retard diffusion.

23. The method of claim 20 further comprising:
binding the pad and the layer of material to retard diffusion with a binding material; and
adding a solderable layer of material onto the pad to enhance the solderability of the pad.

24. A method for forming a bump on a ball grid array device comprising:
forming a copper pad on a substrate;
placing a layer of material to retard diffusion of the copper over the copper pad;
placing lead free solder on the copper pad; and

heating the ball grid array device to heat the lead free solder to a liquid state so that the surface tension of the lead free solder forms a ball; and

cooling the ball grid array device.

25. The method of claim 24 further comprising binding the diffusion retarding layer to the copper pad.

26. The method of claim 25 wherein binding the diffusion retarding layer to the copper pad includes placing a binding layer of titanium (Ti) on the copper pad.

27. The method of claim 24 further comprising placing a layer of gold on the diffusion retarding layer to enhance the ability of the pad to receive solder.

28. A ball grid array device comprising:

a substrate including a first major surface, the substrate further including an array of pads made of an electrically conductive material, the array of pads positioned on the first major surface; and

solder placed on at least one of the array of pads, the solder and the pad including a intermetallic compound including Ni-Sn (Ni_3Sn_4) and Sn-Fe.

29. The ball grid array device of claim 28 wherein the solder is lead-free.

30. The ball grid array device of claim 28 wherein the pad includes a layer of gold.